REMARKS

The Office Action dated April 11, 2002, has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

By this Amendment, claims 1, 5-10, 14-16, 19 and 23 have been amended. No new matter has been added by the amendments. Accordingly, claims 1-23 are pending in this application and are respectfully submitted for consideration.

Figures 1-2 of the Drawings have been objected to. The Examiner states that Figures 1-2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. The Drawings have been amended per the Examiner's suggestion to add the legend --Prior Art--. Thus, withdrawal of the rejection is respectfully requested.

Claims 6-9 and 15 and 17 are rejected under 35 U.S.C. §112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 6-9, 15 and 17 have been amended as shown on the attached sheet to overcome this rejection. Thus, withdrawal of the rejection is respectfully requested.

Claims 1-6, 8-15 and 17-23 have been rejected under 35 U.S.C. §102(e) as being anticipated by Ilkbahar (U.S. Patent No. 6,026,456). The rejection is respectfully traversed because Ilkbahar fails to disclose, teach or suggest each and every element recited in the rejected claims.

For example, Ilkbahar fails to disclose, teach or suggest a first termination resistor block have a first plurality of transistors which include at least one diode-

connected transistor, and a second termination resistor block having a second plurality of transistors which include no diode-connected transistor as recited in claims 1, 10, 19 and 23. In addition Ilkbahar fails to disclose teach or suggest a first termination resistor block which differs from the second termination resistor block by including at least one transistor whose gate is connected to its drain as recited in claims 5 and 14 of the present invention. In other words, Ilkbahar does not teach or suggest a symmetric load type termination resistor circuit. Further Ilkbahar does not teach or suggest optionally employing and switching between symmetric load type and transfer gate type termination resistor circuits as accomplished by the above features recited in the present invention.

Ilkbahar merely discloses pull-up devices 530 and 540, which do not have a diode-connected transistor. The pull-up 540 comprises transistors 542, 544 and 546, which are P channel transistors and selectively couple the interface node 555 to Vt according to a control bus 524 (Column 7, lines 51-60). Ilkbahar also discloses that three pull-up termination resistor blocks are selected and operated by gate signals 528, 526 and 524, where a first resistor block has an NMOS transistor 560, a second pull up resistor block 530 has PMOS transistors 532 to 536, and resistor block 540 has NMOS transistors 542 to 546 (Column 7, line 51-Column 8, line 5).

Ilkbahar also discloses that in order to drive a low voltage, the control circuit enables the pulldown 550 and disables the pull-ups 530, 540 and 560. To drive the high voltage, the control circuit enables the pull-up 530 and disables the pulldown 550. The control circuit 520 enables the pull-up 560 and the pull-up 540 to terminate the interface node 555 unless the pulldown is enabled. The control circuit 520 may be

configured to disable the termination pull-ups 540 and 560 at other times (Column 8, lines 49-59). Consequently, there is no teaching or suggestion by Ilkbahar that a first termination resistor block has a first plurality of transistors which include at least one diode-connected transistor, and a second termination resistor block has a second plurality of transistors which include no diode-connected transistor as recited in claims 1, 10, 19 and 23 of the present invention. In addition Ilkbahar fails to disclose teach or suggest a first termination resistor block which differs from the second termination resistor block by including at least one transistor whose gate is connected to its drain as recited in claims 5 and 14 of the present invention.

Therefore, claims 1, 5, 10, 14, 19, 23 are patentable over Ilkbahar. Thus withdrawal of the rejection of these claims under 35 U.S.C. 102(e) in view of Ilkbahar is respectfully requested. Claims 2-4, 8-9, 11-14, 17-18, and 20-22 depend from claims 1, 5, 10, 14 and 19 respectively. Therefore, these claims patentable for the same reasons as discussed above. Thus withdrawal of the rejection of claims 2-4, 8-9, 11-14, 17-18, and 20-22 under 35 U.S.C. 102(e) in view of Ilkbahar is respectfully requested.

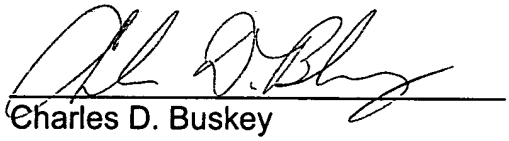
Claims 7 and 16 are been rejected under 35 U.S.C. §103 as being unpatentable over Ilkbahar. The rejection is respectfully traversed because Ilkbahar fails to disclose teach or suggest all the features recited in the rejected claims.

Claims 7 and 16 depend from claims 4 and 13 respectively. Consequently, claims 7 and 16 are patentable for at least the same reasons as discussed above with respect to claims 4 and 13. Thus, withdrawal of the rejection of claims 7 and 16 under 35 U.S.C. §103 is respectfully requested.

Should the Examiner feel that further action is required to place this application in better condition for allowance, the Examiner is requested to contact the undersigned at the telephone number listed below.

In the event this paper is not being timely filed, the Applicant respectfully petitions for an appropriate extension time period. Any fees for such an extension of time, together with any additional fees, may be charged to counsel's Deposit Account No. 01-2300 making reference to Attorney Docket No. 100021-00062.

Respectfully submitted,



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Enclosures:
Marked-Up Version of the Claims

MARKED UP COPY OF THE CLAIMS

1. (Twice Amended) A termination resistor circuit, provided in an interface circuit through which signals are transferred, comprising:

a first termination resistor block having a first plurality of transistors, the first plurality of transistors including at least one diode-connected transistor [with a same logic voltage being applied to gates of the transistors of said first termination resistor block] ; and

a second termination resistor block having a second plurality of transistors, the second plurality of transistors including no diode-connected transistor [with different logic voltages being applied to gates of the transistors of said second termination resistor block, which differs in configuration from said first termination resistor block], and wherein:

said termination resistor circuit is switched between said first termination resistor block and said second termination resistor block.

5. (Twice Amended) A termination resistor circuit provided in an interface circuit through which signals are transferred [via a transmission line] comprising:

a first termination resistor block [having a plurality of transistors of a same conductivity type]; and

a second termination resistor block, [which differs in configuration from said first termination resistor block,] wherein

said first termination resistor block [operates and maintains a specific resistance value when a signal of said transmission line is near a supply voltage] differs from said

second termination block by including at least one transistor whose gate is connected to its drain; and

said [second] termination resistor [block comprises a first conductivity type transistor which does not operate near a first supply voltage, and a second conductivity type transistor which does not operate near a second supply voltage, and]

[said termination resistor] circuit is switched between said first termination resistor block and said second termination resistor block.

6. (Twice Amended) The termination resistor circuit as claimed in claim 4, wherein said first termination resistor block has first and second transistors and said first and second transistors are chosen to have a size for [each of] said first termination resistor [blocks] block so that said [plurality of] first termination resistor [blocks have] block has a respectively chosen [weights] weight.

7. (Amended) The termination resistor circuit as claimed in claim 4, wherein said [third and fourth] transistors of said first and second termination resistor blocks are chosen to be substantially equal in size for each of said first and second termination resistor blocks so that said [plurality of] first and second termination resistor blocks have the same weight.

8. (Twice Amended) The termination resistor circuit as claimed in claim 4, wherein said [third and fourth] transistors for said first and second termination transistor blocks are chosen to have a size for each of said first and second termination resistor

blocks so that said [plurality of] first and second termination resistor blocks have respectively chosen weights.

9. (Amended) The termination resistor circuit as claimed in claim 3, wherein [said] a first transistor and [said] a third transistor of said plurality of transistors of said first and second termination resistor blocks respectively are replaced by one common transistor.

10. (Twice Amended) A signal transmission system comprising:

a transmitting circuit for transmitting a signal;

a transmission line for transmitting the signal output from said transmitting circuit;

a receiving circuit for receiving the signal transmitted from said transmitting circuit through said transmission line; and

a termination resistor circuit connected to said transmission line and provided in an interface circuit through which signals are transferred, wherein said termination resistor circuit comprises:

a first termination resistor block having a first plurality of transistors, the first plurality of transistors including at least one diode-connected transistor [with a same logic voltage being applied to gates of the transistors of said first termination resistor block] ; and

a second termination resistor block having a second plurality of transistors, the second plurality of transistor including no diode-connected transistor [with different logic voltages being applied to gates of the transistors of said second termination resistor

block, which differs in configuration from said first termination resistor block], and wherein:

said termination resistor circuit is switched between said first termination resistor block and said second termination resistor block.

14. (Twice Amended) A signal transmission system comprising:

a transmitting circuit for transmitting [out] a signal;

a transmission line for transmitting [therethrough] the signal output from said transmitting circuit;

a receiving circuit for receiving the signal transmitted from said transmitting circuit through said transmission line; and

a termination resistor circuit connected to said transmission line and provided in an interface circuit through which signals are transferred, wherein said termination resistor circuit comprises:

a first termination resistor block [having a plurality of transistors of a same conductivity type]; and

a second termination resistor block, [which differs in configuration from said first termination resistor block, and] wherein:

said first termination resistor block <u>differs from said second termination resistor block by including at least one transistor whose gate is connected to its drain</u> [operates and maintains a specific resistance value when a signal of said transmission line is near a supply voltage]; and

[said second termination resistor comprises a first conductivity type transistor

which does not operate near a first supply voltage, and a second conductivity type transistor which does not operate near a second supply voltage, and wherein,]

said termination resistor circuit is switched between said first termination resistor block and said second termination resistor block.

15. (Twice Amended) The signal transmission system as claimed in claim 13, wherein [said] first and second transistors are chosen to have a size for each of said first and second termination resistor blocks so that said [plurality of] first and second termination resistor blocks have respectively chosen weights.

16. (Amended) The signal transmission system as claimed in claim 13, wherein [said] third and fourth transistors are chosen to be substantially equal in size for each of said first and second termination resistor blocks so that said [plurality of] first and second termination resistor blocks have the same weight.

19. (Twice Amended) A signal transmission system comprising:

a transmission line for transmitting a signal;

a receiving circuit for receiving the signal transmitted through said transmission line; and

a termination resistor circuit connected to said transmission line and provided in an interface circuit through which signals are transferred, wherein said termination resistor circuit comprises:

a first termination resistor block having a first plurality of transistors, the first

plurality of transistors including at least one diode-connected transistor [with a same logic voltage being applied to gates of the transistors of said first termination resistor block]; and

a second termination resistor block having a second plurality of transistors [with different logic voltages being applied to gates of the transistors of said second termination resistor block], the second plurality of transistors including no diode-connected transistor, [which differs in configuration from said first termination resistor block,] and wherein:

said termination resistor circuit is switched between said first termination resistor block and said second termination resistor block.

23. (Twice Amended) A signal transmission system comprising:

a transmitting circuit for transmitting [out] a signal;

a transmission line for transmitting [therethrough] the signal output from said transmitting circuit;

a receiving circuit for receiving the signal transmitted from said transmitting circuit through said transmission line; and

a termination resistor circuit connected to said transmission line and provided in an interface circuit through which signals are transferred, wherein said termination resistor circuit comprises:

a first termination resistor block having a first plurality of transistors, the first plurality of transistors including at least one diode-connected transistor [the same logic voltage being applied to gates of the transistors of said first termination resistor block];

and

a second termination resistor block having a second plurality of transistors, the second plurality of transistors including no diode-connected transistor[with different logic voltages being applied to gates of the transistors of said second termination resistor block, which differs in configuration from said first termination resistor block], and wherein:

said termination resistor circuit is switched between said first termination resistor block and said second termination resistor block.